

## HARDWARE-EFFICIENT IMPLEMENTATION OF DYNAMIC ELEMENT MATCHING IN SIGMA-DELTA DAC'S

### Abstract

A data shuffler apparatus for shuffling input bits includes a plurality of bit shufflers each inputting corresponding two bits  $x_0$  and  $x_1$  of the input bits and outputting a vector  $\{x_0', x_1'\}$  such that a number of 1's at bit  $x_0'$  over time is within  $\forall 1$  of a number of 1's at bit  $x_1'$ . At least two 4-bit vector shufflers input the vectors  $\{x_0', x_1'\}$ , and output 4-bit vectors, each 4-bit vector corresponding to a combination of corresponding two vectors  $\{x_0', x_1'\}$  produced by the bit shufflers, such that the 4-bit vector shufflers operate on the vectors  $\{x_0', x_1'\}$  in the same manner as the bit shufflers operate on the bits  $x_0$  and  $x_1$ . The current state of the bit shufflers is updated based on a next state of the 4-bit vector shufflers.

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